

## ABSTRACT OF THE DISCLOSURE

A memory cell with at least two detectable states among which is an unprogrammed state, comprising, in series between two terminals of application of a read voltage, at least one first branch comprising: a pre-read stage comprising, in parallel, two switchable resistors having different values with a first predetermined difference; and a programming stage formed of a polysilicon programming resistor, a terminal of the programming resistor being accessible by a programming circuit capable of causing an irreversible decrease in its value.

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